WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a heavily-doped diffusion layer formed, by using a dopant ion having a relatively large mass number, in an epitaxial region of silicon included in at least an upper portion of an epitaxial semiconductor substrate.

2. The semiconductor device of Claim 1,

wherein said epitaxial region has a <110>-oriented zone axis.

3. The semiconductor device of Claim 1,

wherein said heavily-doped diffusion layer is formed by using, as said dopant ion, an indium ion at a dose of 5 x $10^{13}/cm^{-2}$ or more.

4. The semiconductor device of Claim 1,

wherein said heavily-doped diffusion layer corresponds to a pocket heavily-doped diffusion layer of a MIS semiconductor device, and

said MIS semiconductor device includes:

a gate electrode formed above said epitaxial region with a gate insulating film sandwiched therebetween;

a source/drain heavily-doped diffusion layer of a first conductivity type formed in a source/drain region of said epitaxial region at a distance from a region below a side face of said gate electrode;

an extension heavily-doped diffusion layer of the

first conductivity type formed in said epitaxial region between said source/drain heavily-doped diffusion layer and said region below the side face of said gate electrode and having shallower junction than said source/drain heavily-doped diffusion layer; and

said pocket heavily-doped diffusion layer of a second conductivity type formed in said epitaxial region under said extension heavily-doped diffusion layer.

5. The semiconductor device of Claim 4,

wherein said extension heavily-doped diffusion layer is formed by using an antimony ion as a dopant.

6. A semiconductor device comprising:

a heavily-doped diffusion layer formed, by using a dopant ion having a relatively large mass number, in a semiconductor substrate having a <110>-oriented zone axis.

7. The semiconductor device of Claim 6,

wherein said heavily-doped diffusion layer is formed by using, as said dopant ion, an indium ion at a dose of 5 x $10^{13}/cm^{-2}$ or more.

8. The semiconductor device of Claim 6,

wherein said heavily-doped diffusion layer corresponds to a pocket heavily-doped diffusion layer of a MIS semiconductor device, and

said MIS semiconductor device includes:

a gate electrode formed above said semiconductor

substrate with a gate insulating film sandwiched therebetween;

a source/drain heavily-doped diffusion layer of a first conductivity type formed in a source/drain region of said semiconductor substrate at a distance from a region below a side face of said gate electrode;

an extension heavily-doped diffusion layer of the first conductivity type formed in said semiconductor substrate between said source/drain heavily-doped diffusion layer and said region below the side face of said gate electrode and having shallower junction than said source/drain heavily-doped diffusion layer; and

said pocket heavily-doped diffusion layer of a second conductivity type formed in said semiconductor substrate under said extension heavily-doped diffusion layer.

9. The semiconductor substrate of Claim 8,

wherein said extension heavily-doped diffusion layer is formed by using an antimony ion as a dopant.

10. A method for fabricating a semiconductor device comprising:

a step of forming a heavily-doped diffusion layer by implanting a dopant ion having a relatively large mass number into an epitaxial region of silicon included in at least an upper portion of an epitaxial semiconductor substrate.

11. The method for fabricating a semiconductor device

of Claim 10,

wherein said epitaxial region has a <110>-oriented zone axis.

12. The method for fabricating a semiconductor device of Claim 10,

wherein said heavily-doped diffusion layer is formed by using, as said dopant ion, an indium ion at a dose of 5 x $10^{13}/cm^{-2}$ or more.

13. The method for fabricating a semiconductor device of Claim 10,

wherein said heavily-doped diffusion layer corresponds to a pocket heavily-doped diffusion layer of a MIS semiconductor device, and

the method for fabricating said MIS semiconductor device includes the steps of:

forming a gate electrode above said epitaxial region with a gate insulating film sandwiched therebetween;

forming a first dopant layer to be used as said pocket heavily-doped diffusion layer by implanting a first dopant of a first conductivity type corresponding to said dopant ion into said epitaxial region with said gate electrode used as a mask;

forming a second dopant layer to be used as an extension heavily-doped diffusion layer by implanting a second dopant of a second conductivity type into said

epitaxial region to have shallower junction than said first dopant layer with said gate electrode used as a mask; and

forming a sidewall on a side face of said gate electrode, and forming a third dopant layer to be used as a source/drain heavily-doped diffusion layer by implanting a third dopant of the second conductivity type into said epitaxial region to have deeper junction than said second dopant layer with said gate electrode and said sidewall used as a mask.

14. The method for fabricating a semiconductor device of Claim 13, further comprising a step of forming a fourth dopant layer to be used as a channel diffusion layer by implanting a fourth dopant of the first conductivity type into said epitaxial region before forming said gate electrode.

15. The method for fabricating a semiconductor device of Claim 13,

wherein said second dopant is an antimony ion.

16. A method for fabricating a semiconductor device comprising:

a step of forming a heavily-doped diffusion layer by implanting a dopant ion having a relatively large mass number into a semiconductor substrate under conditions for suppressing dislocation loop defects caused in said semiconductor substrate.

17. The method for fabricating a semiconductor device

of Claim 16,

wherein said heavily-doped diffusion layer is formed by using, as said dopant ion, an indium ion at a dose of 5 x $10^{13}/cm^{-2}$ or more.

18. The method for fabricating a semiconductor device of Claim 16,

wherein said dopant ion is implanted at a current density of approximately 100 $\mu A/cm^2$ or less.

19. The method for fabricating a semiconductor device of Claim 16,

wherein said dopant ion is implanted at an angle of approximately 30 degrees or more against a vertical direction to a substrate surface of said semiconductor substrate.

20. The method for fabricating a semiconductor device of Claim 16,

wherein said heavily-doped diffusion layer corresponds to a pocket heavily-doped diffusion layer of a MIS semiconductor device, and

the method for fabricating said MIS semiconductor device includes the steps of:

forming a gate electrode above said semiconductor substrate with a gate insulating film sandwiched therebetween;

forming a first dopant layer to be used as said pocket heavily-doped diffusion layer by implanting a first

dopant of a first conductivity type corresponding to said dopant ion into said semiconductor substrate with said gate electrode used as a mask;

forming a second dopant layer to be used as an extension heavily-doped diffusion layer by implanting a second dopant of a second conductivity type into said semiconductor substrate to have shallower junction than said first dopant layer with said gate electrode used as a mask; and

forming a sidewall on a side face of said gate electrode, and forming a third dopant layer to be used as a source/drain heavily-doped diffusion layer by implanting a third dopant of the second conductivity type into said semiconductor substrate to have deeper junction than said second dopant layer with said gate electrode and said sidewall used as a mask.

21. The method for fabricating a semiconductor device of Claim 20, further comprising a step of forming a fourth dopant layer to be used as a channel diffusion layer by implanting a fourth dopant of the first conductivity type into said semiconductor substrate before forming said gate electrode.

22. The method for fabricating a semiconductor device of Claim 20,

wherein said second dopant is an antimony ion.

23. A method for fabricating a semiconductor device comprising:

a step of forming a heavily-doped diffusion layer by implanting a dopant ion having a relatively large mass number into a semiconductor substrate having a <110>-oriented zone axis.

24. The method for fabricating a semiconductor device of Claim 23,

wherein said heavily-doped diffusion layer is formed by using, as said dopant ion, an indium ion at a dose of 5 x $10^{13}/cm^{-2}$ or more.

25. The method for fabricating a semiconductor device of Claim 23,

wherein said heavily-doped diffusion layer corresponds to a pocket heavily-doped diffusion layer of a MIS semiconductor device, and

the method for fabricating said MIS semiconductor device includes the steps of:

forming a gate electrode above said semiconductor substrate with a gate insulating film sandwiched therebetween;

forming a first dopant layer to be used as said pocket heavily-doped diffusion layer by implanting a first dopant of a first conductivity type corresponding to said dopant ion into said semiconductor substrate with said gate

electrode used as a mask;

forming a second dopant layer to be used as an extension heavily-doped diffusion layer by implanting a second dopant of a second conductivity type into said semiconductor substrate to have shallower junction than said first dopant layer with said gate electrode used as a mask; and

forming a sidewall on a side face of said gate electrode, and forming a third dopant layer to be used as a source/drain heavily-doped diffusion layer by implanting a third dopant of the second conductivity type into said semiconductor substrate to have deeper junction than said second dopant layer with said gate electrode and said sidewall used as a mask.

26. The method for fabricating a semiconductor device of Claim 25, further comprising a step of forming a fourth dopant layer to be used as a channel diffusion layer by implanting a fourth dopant of the first conductivity type into said semiconductor substrate before forming said gate electrode.

27. The method for fabricating a semiconductor device of Claim 25,

wherein said second dopant is an antimony ion.

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